Sub Code: R2321044 **R23** **Set No. 1**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY- GURAJADA VIZIANAGARAM**
**II B. Tech I Semester Regular Examinations, November – 2024**
**DIGITAL CIRCUIT DESIGN**
**(ECE)**

**Time: 3 hours** **Max. Marks: 70**

***Question paper consists of Part A, Part B.***
***Part A is compulsory, Answer all questions.***
***In Part B, Answer any one question from each unit.***
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**PART-A** (20 Marks)

| | | | |
|---|---|---|---|
| 1 | a) | Convert (0.513)10 to octal. | [2] |
| | b) | Find 2's compliment of 10001000 | [2] |
| | c) | Draw the truth table of full adder. | [2] |
| | d) | Give the K-Map of the function F= ∑{1,2,4,6,7} | [2] |
| | e) | What are the types of counters? | [2] |
| | f) | Draw the master slave JK Flip Flop | [2] |
| | g) | What are the Capabilities of FSM? | [2] |
| | h) | Draw the block diagram of Mealy FSM | [2] |
| | i) | Write VERILOG HDL Code of a NAND Gate | [2] |
| | j) | Write VERILOG HDL Code of a 2X1 MUX | [2] |

**PART-B** (50 Marks)

**Unit-1**

| | | | |
|---|---|---|---|
| 2 | a) | Perform subtraction on the given unsigned binary numbers using the 2's complement of the Subtrahend. Where the result should be negative, find its 2's complement and affix a minus sign.<br>(a) 10011 - 10010 (b) 100010 - 100110 | [5] |
| | b) | Find all the prime implicants for the following Boolean functions, and determine which are essential:<br>(a) $F(w, x, y, z) = \sum (0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$<br>(b) $F(A, B, C, D) = \sum (0, 2, 3, 5, 7, 8, 10, 11, 14, 15)$ | [5] |

(OR)

| | | | |
|---|---|---|---|
| 3 | a) | Simplify the following Boolean functions $T1$ and $T2$ to a minimum number of literals: | [5] |

| A | B | C | $T_1$ | $T_2$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 |

| | | | |
|---|---|---|---|
| | b) | Convert the following<br>i. (AC) 16 =( ) 10<br>ii. (132.44) 10 =( ) 2<br>iii. (200) 10 =( ) 8 | [5] |

**Unit-2**

4 a) Implement the given function using multiplexer. [5]
$f(A,B,C,D) = \sum m\ (0,1,2,3,5,7,8,9,10,11,12,13,15)$

b) Draw the logic diagram of priority encoder and explain in detail its operation. [5]

(OR)

5 a) Derive the state tables for the 4 bit ring counter [5]
b) Explain the working of 3-bit bi-directional shift register with the help of diagram? [5]

**Unit-3**

6 a) Explain the differences among a truth table, a state table, a characteristic table, and an Excitation table. Also, explain the difference among a Boolean equation, a state equation, A characteristic equation, and a flip-flop input equation. [10]

(OR)

7 a) Derive the state tables for the 4 bit Johnson counter [5]
b) Design a Mod 12 synchronous Counter [5]

**Unit-4**

8 a) Give the comparison between Moore machine and Mealy machine [5]
b) Design a sequence detector to detect a sequence 1010. [5]

(OR)

9 a) For the state table given below find the equivalence partition and a corresponding reduced machine. [5]

| PS | NS,Z | |
|---|---|---|
| | X=0 | X=1 |
| A | D,0 | A,1 |
| B | F,1 | C,1 |
| C | D,0 | F,1 |
| D | C,0 | E,1 |
| E | C,1 | D,1 |
| F | D,1 | D,1 |

b) Draw and Explain Basic structure of CPLD [5]

**Unit-5**

10 a) Explain with examples the different levels of design description in Verilog. [5]
b) Define and explain the following terms relevant to Verilog HDL with example. [5]
1. Module 2. Test bench

(OR)

11 a) Write Verilog HDL program for 2X4 Decoder in gate level modelling [5]
b) Design 4X1 Mux using data flow modelling [5]

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